WHAT IS CLAIMED IS:

1. A semiconductor package in which a semiconductor chip, a die pad, a die bond material fixing the semiconductor chip on the die pad, LOC type inner leads having their tips extended above the semiconductor chip and metal wires connecting the tips of the LOC type inner leads to electrode pads on the semiconductor chip are sealed with a sealing resin,

wherein outer leads formed successively to the inner leads are protruded outwardly from the sealing resin.

2. A semiconductor package of Claim 1, in which standard type inner leads and metal wires connecting the tips of the standard type inner leads to electrode pads on the semiconductor chip are further sealed with the sealing resin,

wherein outer leads formed successively to the standard type inner leads are protruded outwardly from the sealing resin,

and the LOC type inner leads and the standard type inner leads are arranged on a same plane.

3. A semiconductor package of claim 1, wherein a clearance between the LOC type inner leads and the die pad is set to be larger than a sum of thickness of the semiconductor chip and the die bond material.

4. A semiconductor package of claim 2, wherein the LOC type inner leads and the standard type inner leads are mixedly arranged along at least a side of the semiconductor chip.

5. A semiconductor package of claim 2, wherein the LOC type inner leads are arranged along a side of the semiconductor chip and the standard type inner leads are arranged along another side of the semiconductor chip.

6. A semiconductor package of claim 1, wherein a distance between upper surfaces of the outer leads and the upper surface of the sealing resin is different from a distance between lower surfaces of the outer leads and the lower surface of the sealing resin, and ends of the die pad are exposed in opposed side surfaces of the sealing resin and being on a plane parallel with a plane on which the leads are protruded.

7. A semiconductor package in which at least a semiconductor chip, metal wires, LOC type inner leads having their tips extended above the semiconductor chip and standard type inner leads having their tips arranged outside of periphery of the semiconductor chip are sealed with a sealing resin,

wherein the semiconductor chip has distributed electrode pads distributed and arranged on its upper surface and has at least either central electrode pads rectilinearly provided in a central region of the semiconductor chip or peripheral electrode pads provided along the periphery of the semiconductor chip,

and the LOC type inner leads and the standard type inner leads are arranged on a same plane and mixedly arranged along a side of the semiconductor chip.

8. A method of manufacturing a semiconductor package

comprising;

forming a die pad frame in which die pads are surrounded with a frame,

depressing the die pad to make a displacement between the die pad and the frame,

bonding a semiconductor chip to the die pad with a die bond material,

superposing a lead frame, in which inner leads are surrounded with a frame, on the die pad frame so as to interpose the semiconductor chip between the die pads and the inner leads,

welding the frame of the die pad and the frame of the lead frame together,

sealing the die pad, the semiconductor chip and the inner leads with a sealing resin,

and removing the frame of the die pad and the frame of the lead frame away.